Ultra-low power model-based ASIC design for implantable medical products using HDL Coder

Dean Andersen

Abbott (formerly St. Jude Medical)

Abstract

Model-based design is a path from algorithm to hardware implementation, in this case a full custom mixed-signal integrated circuit for class III implantable medical products. For applications like these, custom integrated circuit die area and power consumption are critical for circuit performance as these parameters translate directly to device size and device longevity.   The model is used for design exploration and algorithm validation. The model is transformed to an RTL description using HDL Coder. The model is refined to meet power and area constraints while iterating between HDL simulation results and model parameters to create the lowest possible power design.   This presentation shows a typical design flow of modelling, validating and implementing an algorithm into a custom ASIC.   The steps in taking the design into an ASIC simulation environment to validate power and area are also presented.

Overview

About Abbott

Motivation for ASIC design

Model-based design

Translation to HDL

HDL verification

Model validation

About Abbott

MEDICAL DEVICES*
38%
of sales

ESTABLISHED PHARMACEUTICALS
15%
of sales

DIAGNOSTICS
18%
of sales

NUTRITION
26%
of sales

* Based on 1 half 2017 results

About Abbott

Cardiac Rhythm Management
- Cardiac resynchronization (CRT)
- Cardiac pacemakers
- Implantable cardioverters defibrillators (ICD)

Insertable Cardiac Monitoring (ICM)
- AF detection

Left Ventricle Assist Device (LVAD)
- Heart failure

Deep Brain Stimulation
- Parkinson's Disease

Spinal Cord Stimulation
- Chronic pain
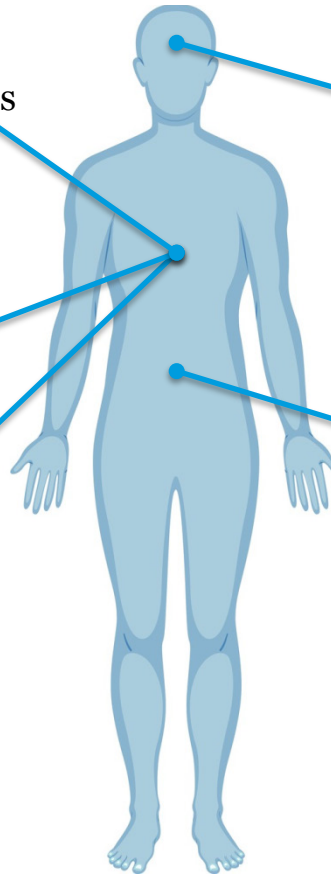
Overview

About Abbott

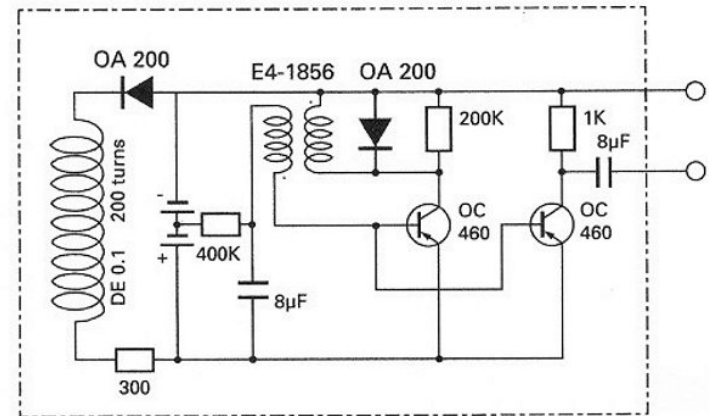**Motivation for ASIC design**

Model-based design

Translation to HDL

HDL verification

Model validation

Motivation for ASIC design

Why custom integrated circuits?

- First implantable pacemaker in 1958
  - Two-transistor blocking oscillator
  - 55 mm in diameter, 16 mm depth
  - Power from 2 rechargeable NiCad batteries
- Modern pacemaker
  - Millions of transistors
  - Sophisticated embedded systems
  - Offering responsive therapy based on individual patient's needs
  - Storing heart electrical activity for retrieval
  - Wireless communication
  - Hundreds of parameters programmable to adjust to patient

LARSSON, B., ELMQVIST, H., RYDÉN, L. and SCHÜLLER, H. (2003), Lessons From the First Patient with an Implanted Pacemaker:. Pacing and Clinical Electrophysiology, 26: 114–124. doi:10.1046/j.1460-9592.2003.00162.x
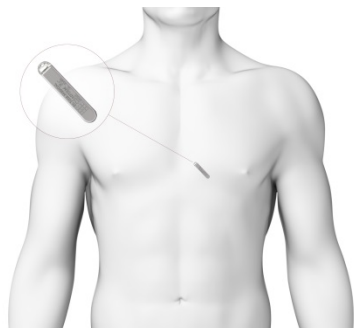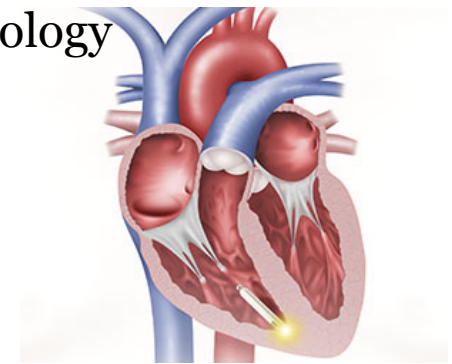
Motivation for ASIC design

Today – large scale of integration driven by small size and longevity

- Longevity has been offset by device sophistication and technology
- Most devices last 7 – 15 years
- Features and algorithms are driving next generation devices

Small size has opened new therapy opportunities

- Leadless pacemakers
- Pulmonary artery pressure
- Insertable cardiac monitors
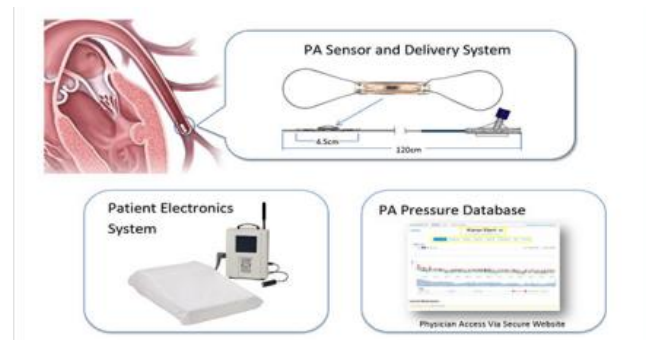
Motivation for ASIC design

Power budgets of pacemakers are extreme!

- Typical implantable device has a primary cell at 2.8V

- Average current of system: 10 – 20 μA

- Peak current 2 – 5 mA

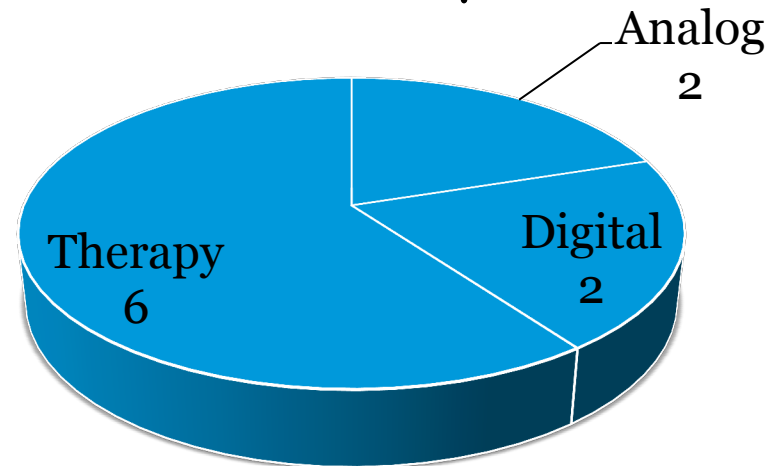- An 11 year device with a 1 A*hr battery

- Miniature package

1 cm^3

- 6mm diameter
- 40 mm length

10 cm^3

- 6mm thick,

Current (μA)

Analog
2

Digital
2

Therapy
6

Overview

About Abbott

Motivation for ASIC design

Model-based design

Translation to HDL

HDL verification

Model validation

Model-based Design

Mixed signal designs

- Analog design
  - Schematic design
  - Simulation
  - Layout
- Digital design
  - HDL (hardware design language)
  - Simulation
  - Synthesis
  - Automated place and route

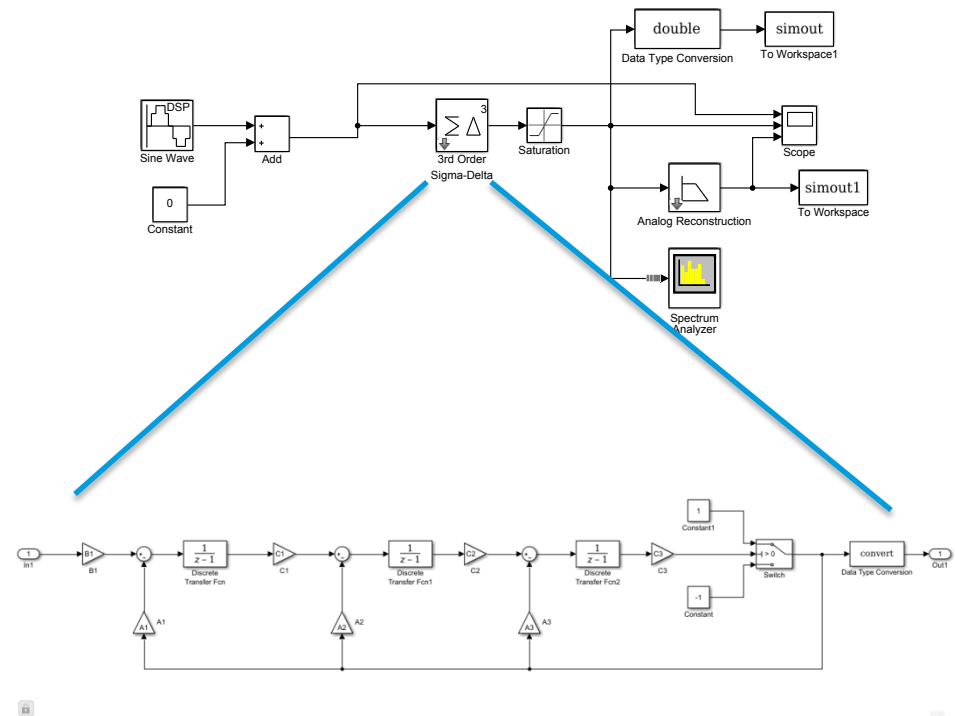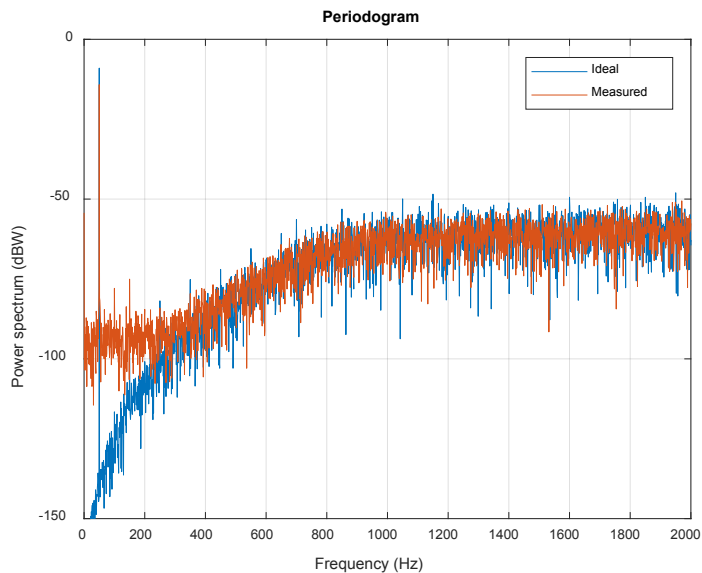Mixed Signal
Simulation
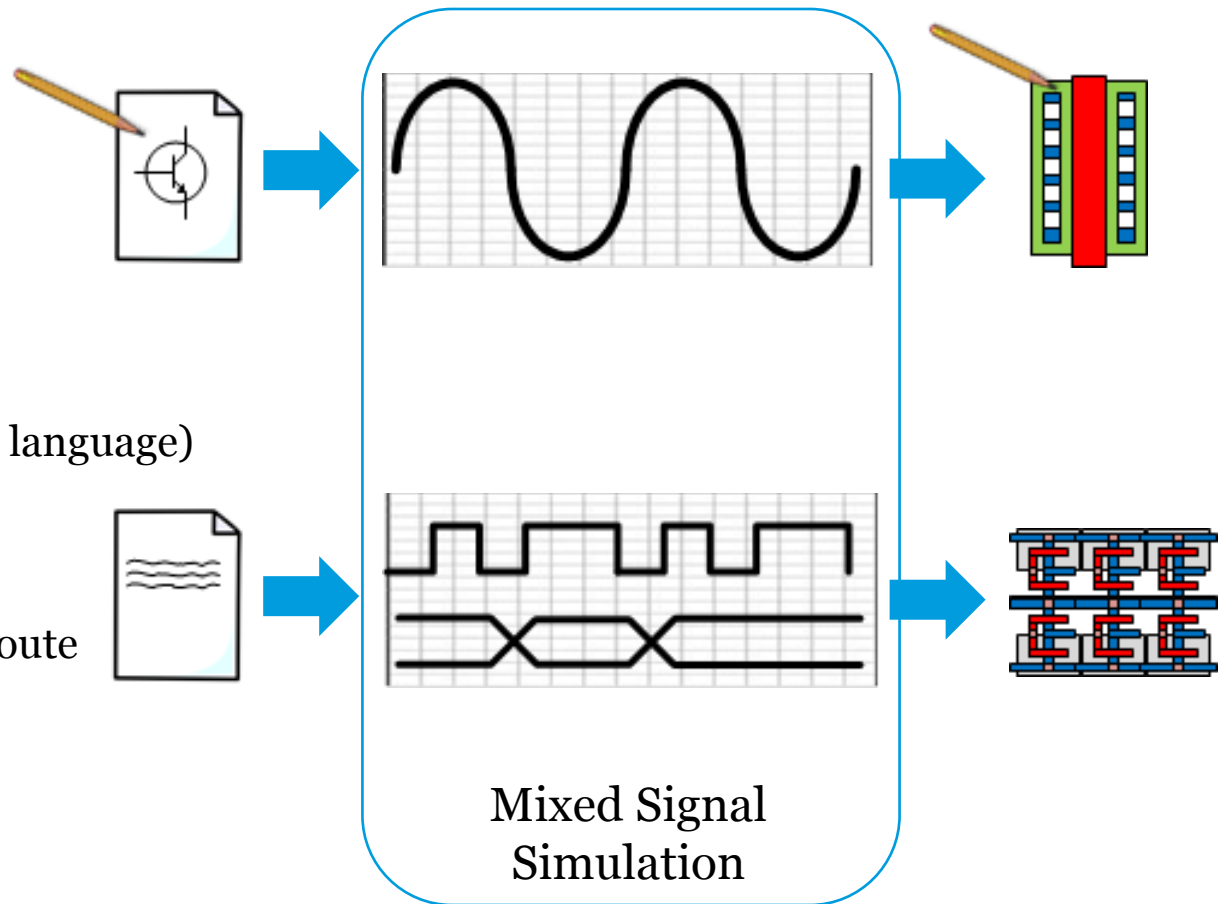
Model-based Design

Simulink® is a mixed-signal simulation environment

- A bridge between analog and digital design
- Familiarity to both analog and digital designers
- Dynamic simulation environment
  - Similar to transient simulation in SPICE
  - Cycle by cycle event modeling similar to digital simulation
- Particularly strong in DSP applications
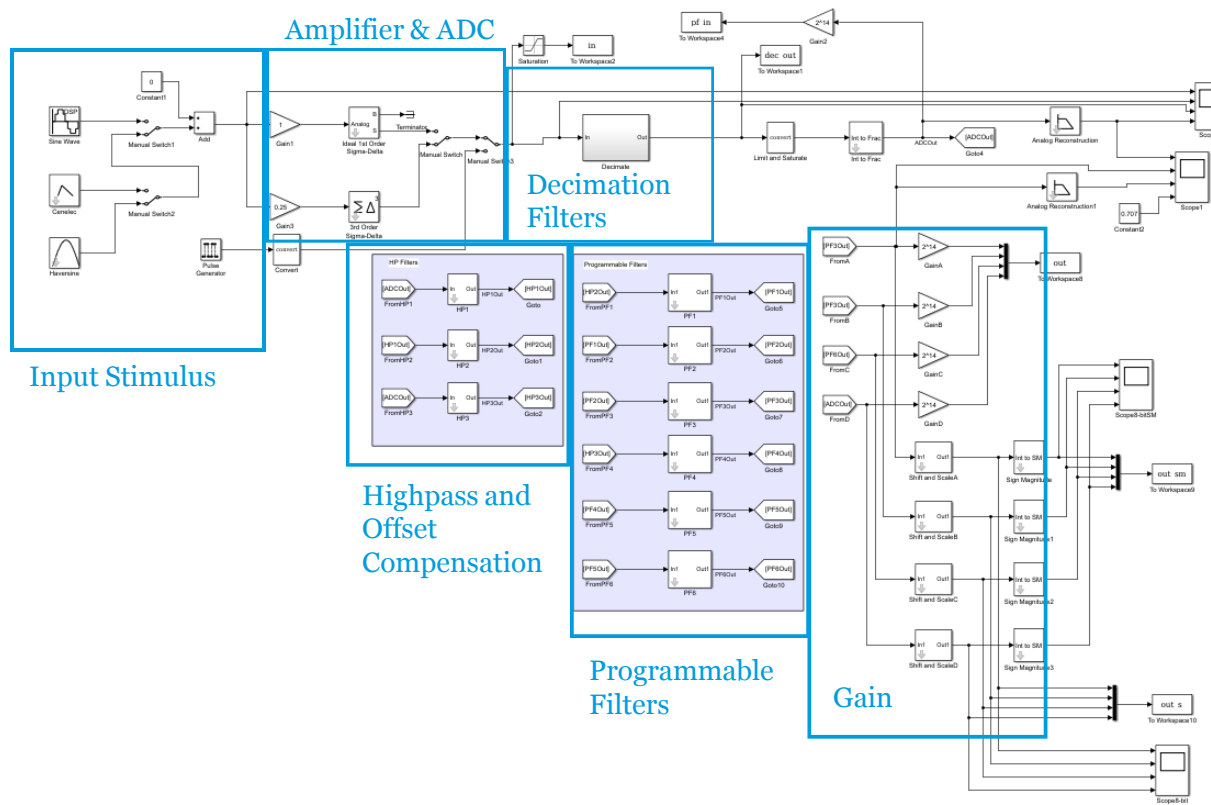
Model-based Design

Example: Sigma-Delta ADC

- Cardiac electrogram sensing
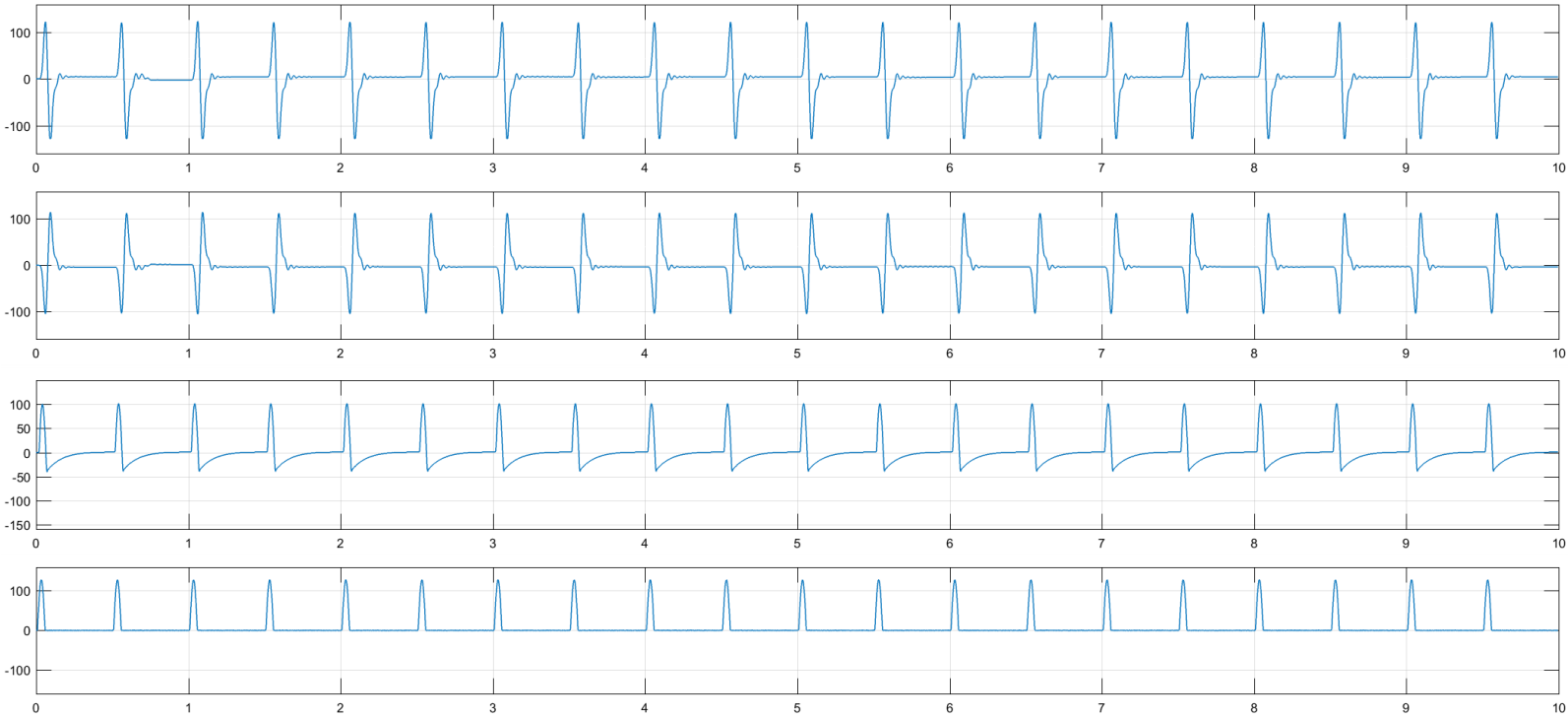- 60 dB SNR
- 3rd Order modulator
- 150 nW power dissipation

Model-based Design

Example complete analog front end model

Input Stimulus

Amplifier & ADC

Decimation Filters

Highpass and Offset Compensation

Programmable Filters

Gain

Model-based Design

Example output

Overview

About Abbott

Motivation for ASIC design

Model-based design

Translation to HDL

HDL verification

Model validation

Translation to HDL

Power vs Configurability

- Trade-off between power and configurability
- General purpose vs. application specific

- General Purpose
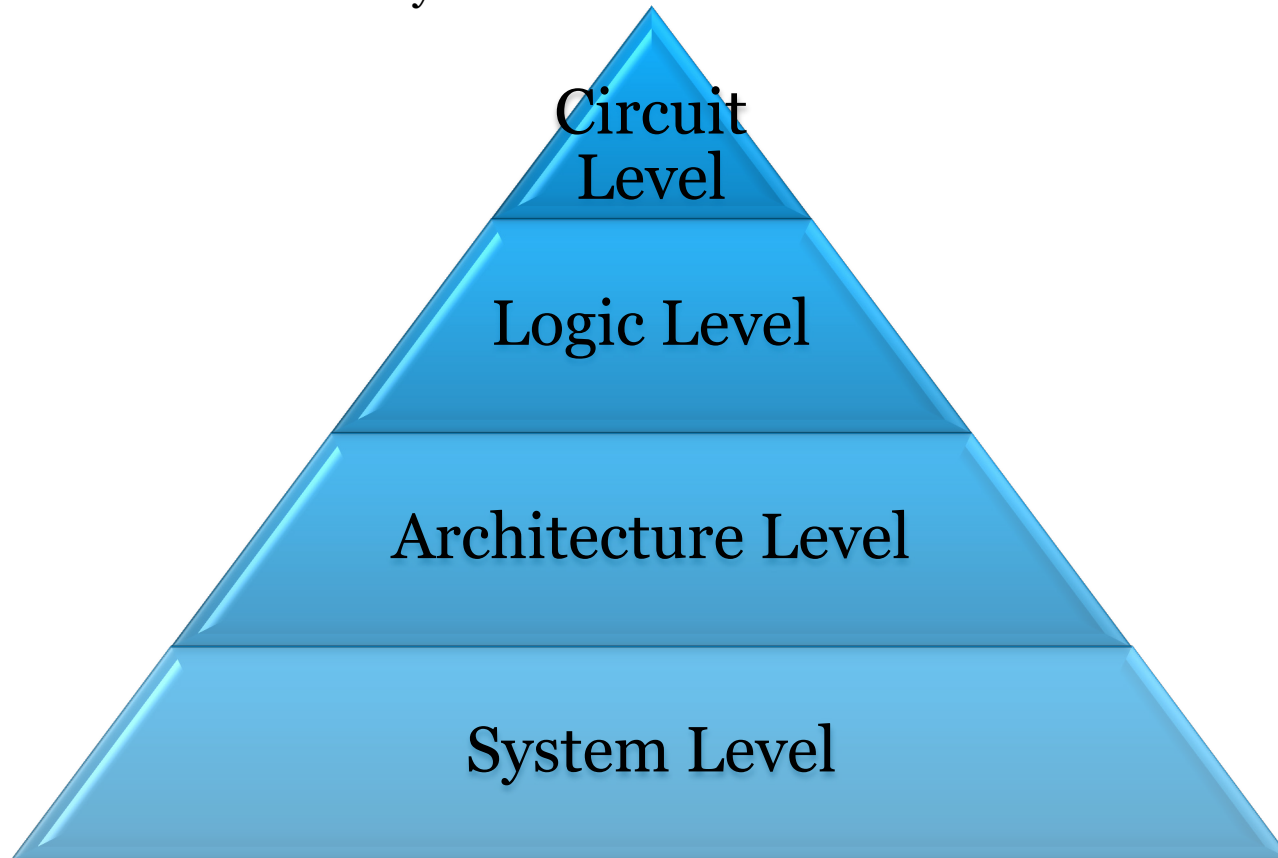- High Configurability
- High Power
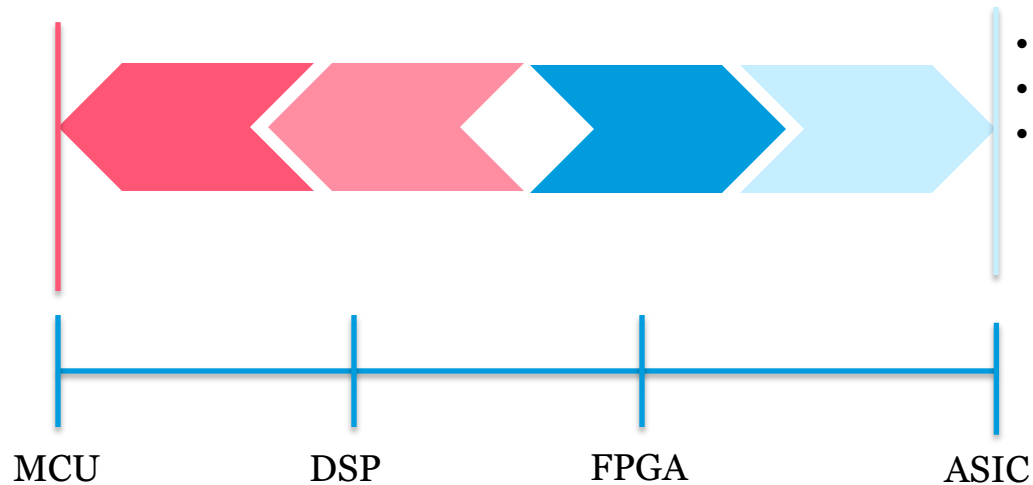
- Application Specific
- Low Configurability
- Low Power

MCU   DSP   FPGA   ASIC
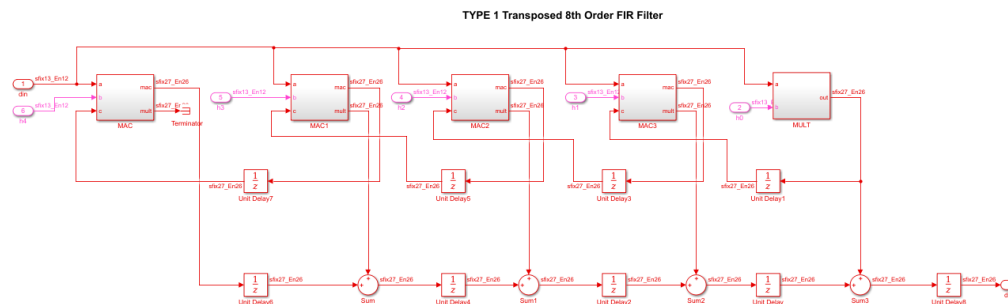
Translation to HDL

Power Triangle

- Most power benefits are at system and architecture levels

Translation to HDL

HDL models optimized for power

- Minimum data paths
  - Sizing and scaling of adders and multipliers
  - Minimized area which minimizes power
  - Parameterizing an RTL model for data path is difficult and requires extensive verification
- Choosing rounding methods
  - Parameterizing an RTL model for data path is difficult and requires extensive verification

TYPE 1 Transposed 8th Order FIR Filter

Translation to HDL

**Architecture exploration**

- Quickly explore various topologies and architectures
- Use MATLAB/Simulink to evaluate performance
- Generate RTL and use simulation tools to evaluate power

HDL Coder

Power Analysis
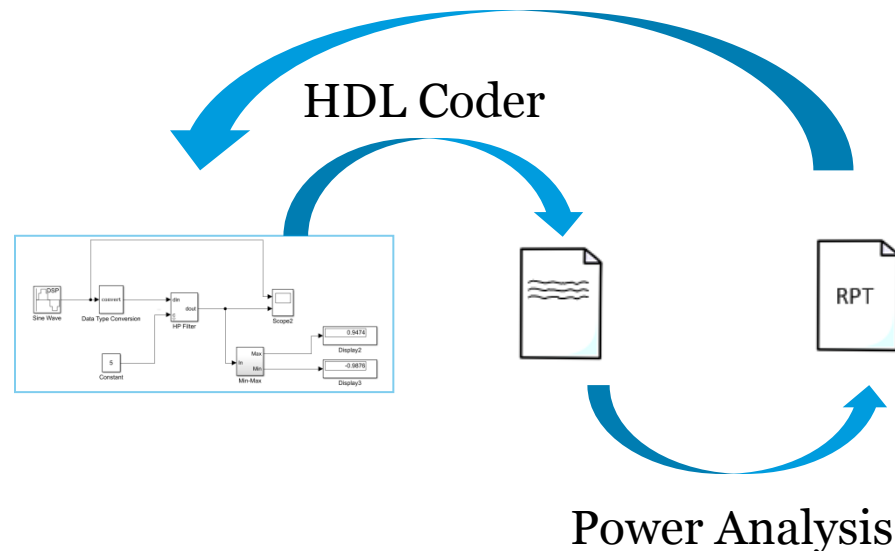
Translation to HDL

Example: Bandpass filter

- Approximately 10 – 30 Hz
- 1000 Hz sample rate
- Three implementations
  - 2nd order Biquad IIR
  - Two 1st order IIR
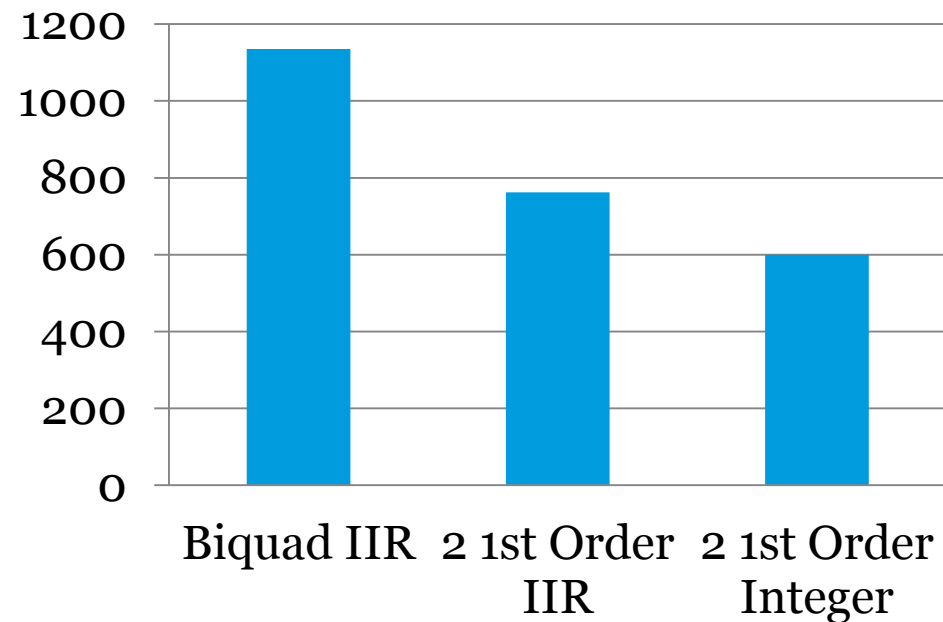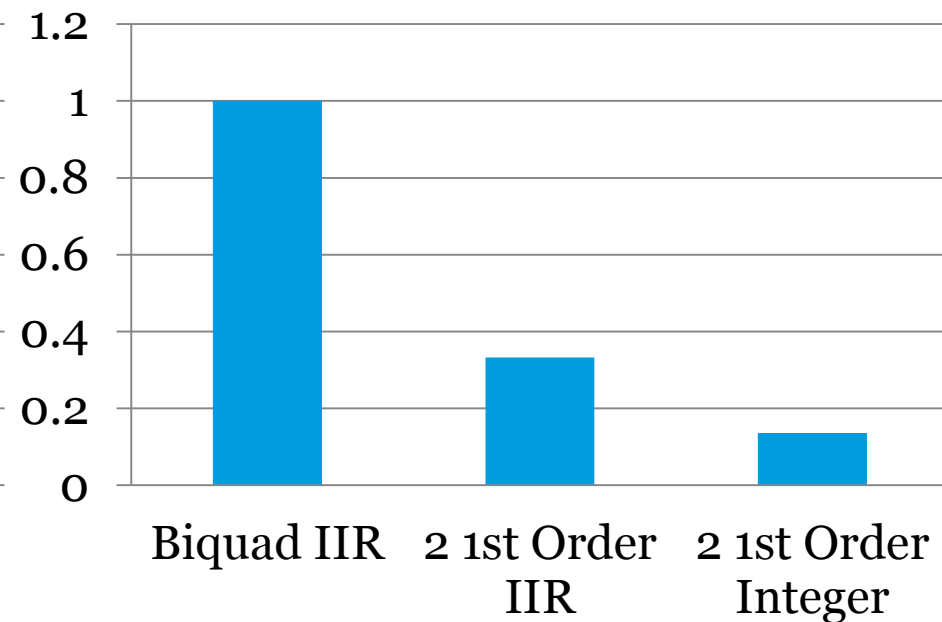 - Two 1st order integer IIR
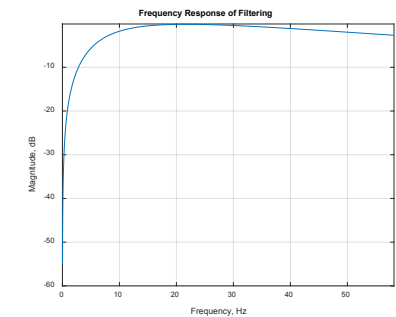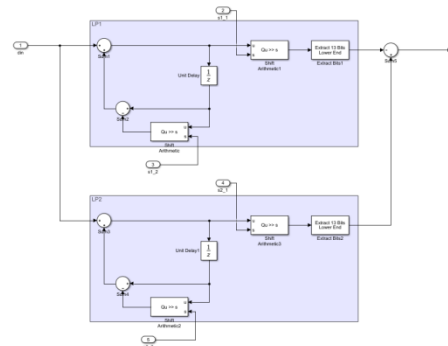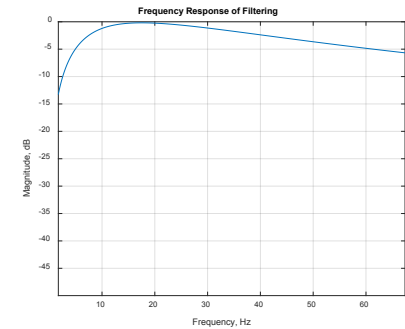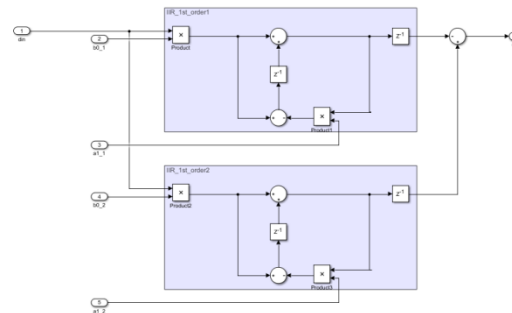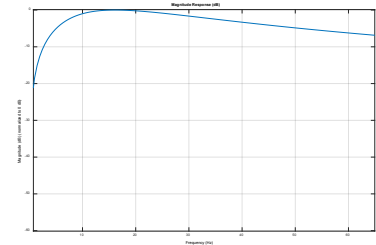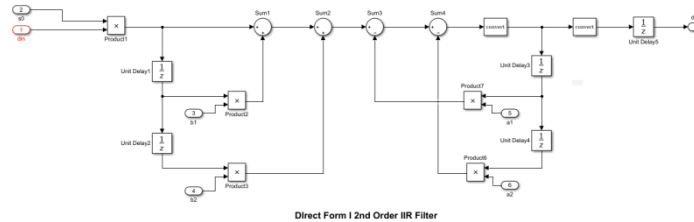
Translation to HDL

Power simulation results

- Technology dependent on ASIC library
- Power estimation using an EDA simulation tool

Energy (nW/MHz)

Relative Area

HDL verification

Verification steps

- Block-level verification
  - Output testbench from HDL coder provides a quick stand-alone verification
- Use HDL model along with data input and expected output
  - This is used to conform to existing testbench environment
  - Can be ported to ASIC top level verification environment
- FPGA rapid prototyping for co-verification
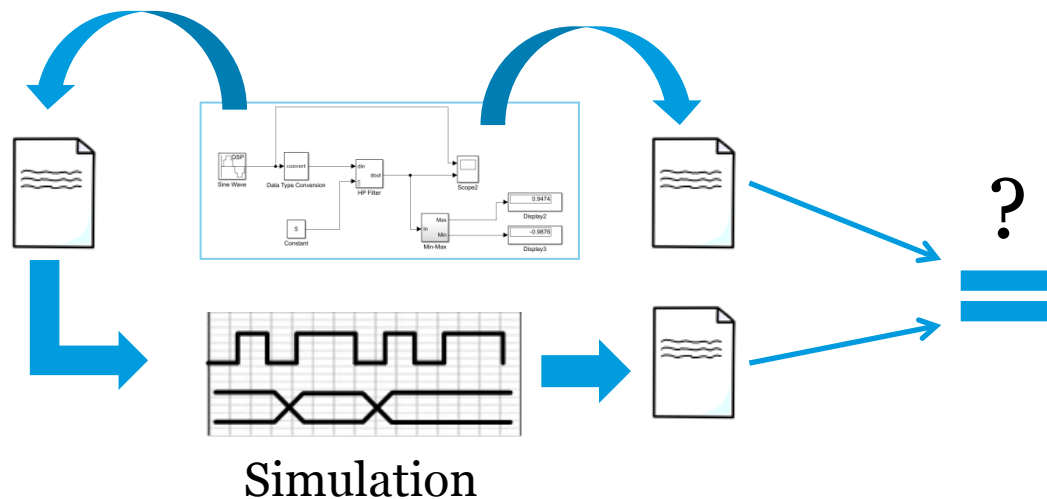
Simulation

Overview

About Abbott

Motivation for ASIC design

Model-based design

Translation to HDL

HDL verification

Model validation

HDL validation

Validation methodology

- Post-silicon
  - Vectors from simulation are run on actual silicon
  - Power is verified
  - Design is tested across parameters such as voltage and temperature
- Model for algorithm development
  - A MATLAB model(s) are created
    - Usually both fixed point and non-fixed point
  - Used by Research and System Engineering to validate behavior
    - For example for CRM devices tested against an extensive library of cardiac arrhythmias
- Animal and human testing

HDL validation

Lifecycle
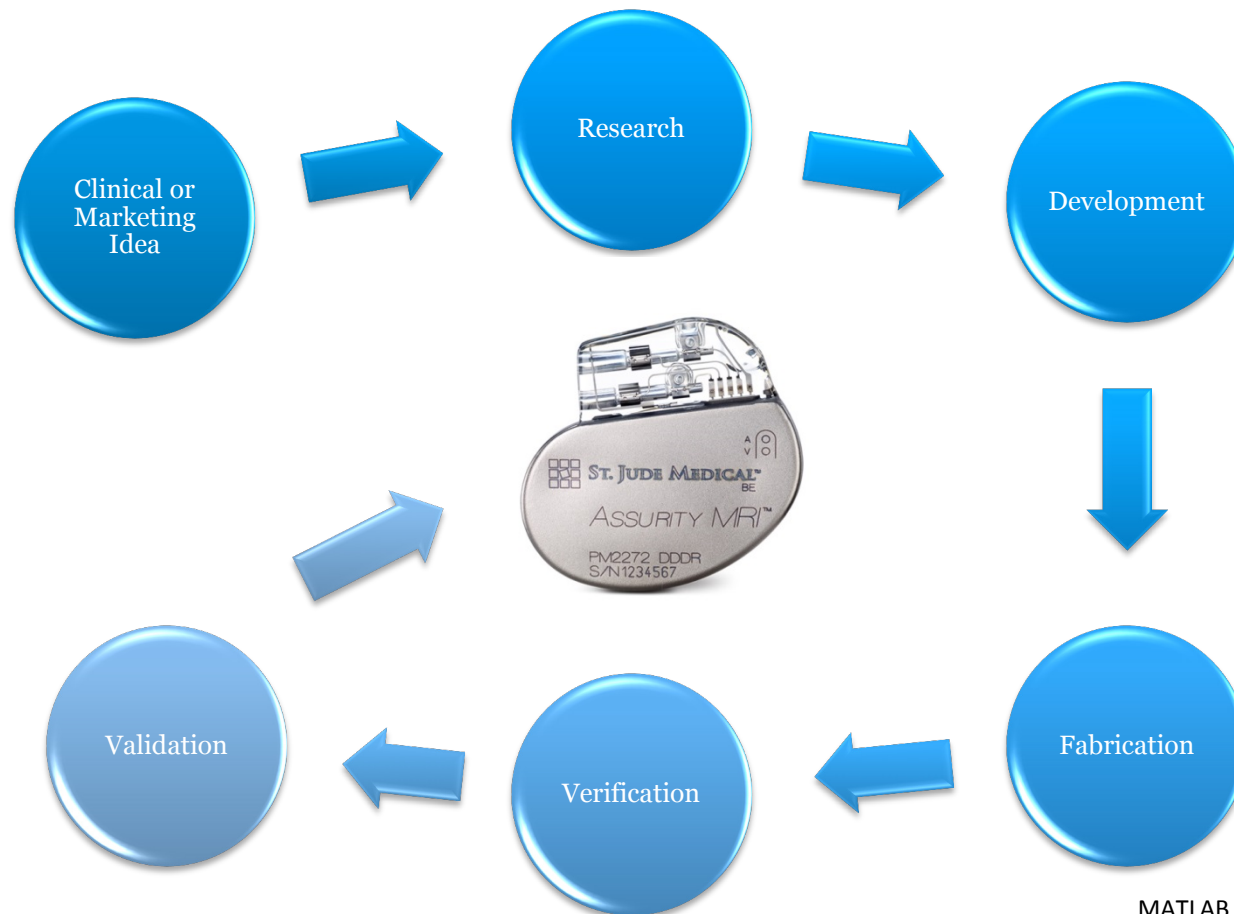
Conclusion

HDL Coder in IC design flow

- Rapid development from architecture to RTL
  - Cuts significant amount of design time
  - Very straightforward datapath optimization for power and performance
  - Making parameterized RTL models is very time consuming and a verification challenge
- Intuitive signal flow centric
- HDL hierarchy is equivalent to model
  - This is necessary for proper evaluation of power
- Simulink model becomes the golden source for verification and validation

THANK YOU

http://www.abbott.com/abbott-stjudemedical-en.html